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PATENT NUMBER and  
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM 10074309	FILING DATE 02/11/2002	CLASS 365	SUBCLASS 194	GAU 2818	EXAMINER LUX
<b>**APPLICANTS:</b> Ahn Young-Man; So Jin-Ho; So Byung-Se; Seo Seung-Jin; 2824					
<b>**CONTINUING DATA VERIFIED:</b> NONE					
<b>** FOREIGN APPLICATIONS VERIFIED:</b> REPUBLIC OF KOREA 2001-8141 02/19/2001					
PG-PUB <input type="checkbox"/> DO NOT PUBLISH <input type="checkbox"/>		RESCIND <input type="checkbox"/>			
Foreign priority claimed <input type="checkbox"/> yes <input type="checkbox"/> no		ATTORNEY DOCKET NO			
35 USC 119 conditions met <input type="checkbox"/> yes <input type="checkbox"/> no		5649-944			
Verified and Acknowledged Examiners's initials					
TITLE : Integrated circuit devices having delay circuits for controlling setup/delay times of data signals that are provided to memory devices and methods of operating same					

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<b>NOTICE OF ALLOWANCE MAILED</b>		<b>CLAIMS ALLOWED</b>	
		Total Claims	Print Claim for O.G.
<b>ISSUE FEE</b>		<b>DRAWING</b>	
Amount Due	Date Paid	Sheets Drwg.	Figs.Drwg. Print Fig.
<input type="checkbox"/> <b>TERMINAL DISCLAMER</b>		<b>Application Examiner</b>	
		<b>PREPARED FOR ISSUE</b>	
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